A DOUBLE GATE METAL-OXIDE-SEMICONDUCTOR STRUCTURE FOR MODULATION OF THE HYPERFINE INTERACTION IN PHOSPHORUS-DOPED SI-DEVICE

BY

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ABSTRACT

In this thesis, we investigate the control of the hyperfine interaction between a conduction electron and a P-impurity nuclear spin in a symmetric metal-oxide semiconductor structure with face-to-face gate oxide layers. We solve the Poisson equation for the device electronics and the Schrödinger equation for the quantum states in the Si - layer by taking into account the nonisotropic effective mass of silicon at each of the six degenerate minima in the conduction band. It is shown that the double gate device leads to better performance, in terms of higher wave function amplitude modulation and consequently higher nuclear magnetic resonance frequency compared to single gate devices for relatively short impurity distances from the oxide layers.

To My Grandmother Shamsi Ravan , Grandfather Javad Rahmansetayesh
& My Parents

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CHAPTER 1

INTRODUCTION

1.1 Lead-In

The development of quantum algorithms for problems unsolved by classical methods such as prime factorization and exhaustive search problems has generated great interest in the realization of quantum computers [1-3]. In fact, the devices as such can perform certain tasks in fewer steps. The core idea comes from the fundamental belief that nature obeys quantum mechanical laws. Alternative to classical systems, the information is stored in a two level system of spins (called qubits). However, in order to realize the devices of quantum computation, a high level of isolation along with a very little consumption of energy (in theory zero) is required. Either of these conditions is very difficult to achieve in real the world. Two main areas of interest which support motivation in realization of quantum computers are the following: first is the development of quantum algorithms and second is the existence of error correcting codes for such machines.

Solid state approaches are most promising [4] because of the compatibility with semiconductor technology and their potential for scalability. The idea comes from incorporation of nuclear spins into an electronic device and detection and control of spin interactions electronically.

Among them, the Kane's scheme is particularly attractive to realize a quantum gate because of its implementation with Si metal oxide semiconductor (MOS) technology and the long decoherence time for electron spin by environmental nuclear spins [5].

1.2 Kane Device

In this scheme, a periodic array of P-impurities is placed under a series of metal gates in the semiconductor layers of a MOS device where single-qubit operations are achieved with the control of the hyperfine interaction between an electron and the P-nucleus by the external electric field of so-called A-gates. Figures 1.1 and 1.2 show the one-dimensional view of the device and the hyperfine control of the wavefunction done electronically through the bias variations applied at A gates.

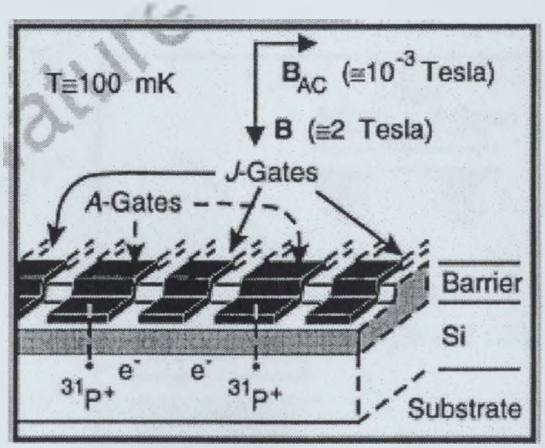


Fig. 1.1: Illustration of two cells in one-dimensional array containing P donors and electrons in Si host, separated by a barrier from metal gates on the surface [5].

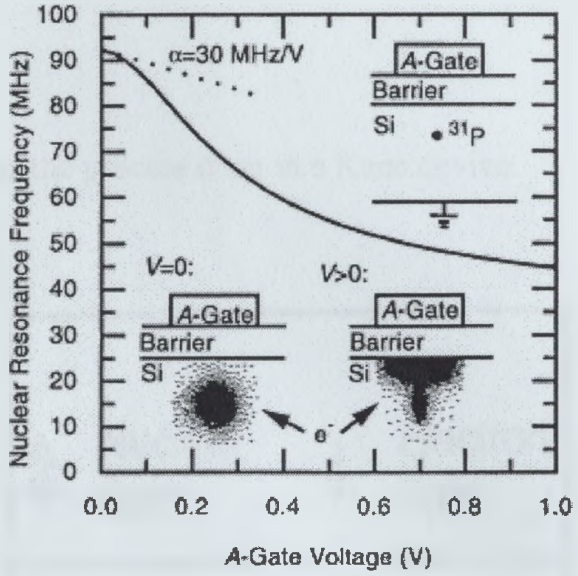


Fig. 1.2: An electric potential applied to an A gate pulls the electron wavefunction away from the donor and towards the barrier, reducing the hyperfine interaction and the resonance frequency of the nucleus. V is the electrostatic potential applied at gate [5].

Electron-mediated exchange coupling between nuclear spin achieves the two qubit operation, controlled by the so-called J-gates positioned at mid-distance between donors as in Fig.1.3.

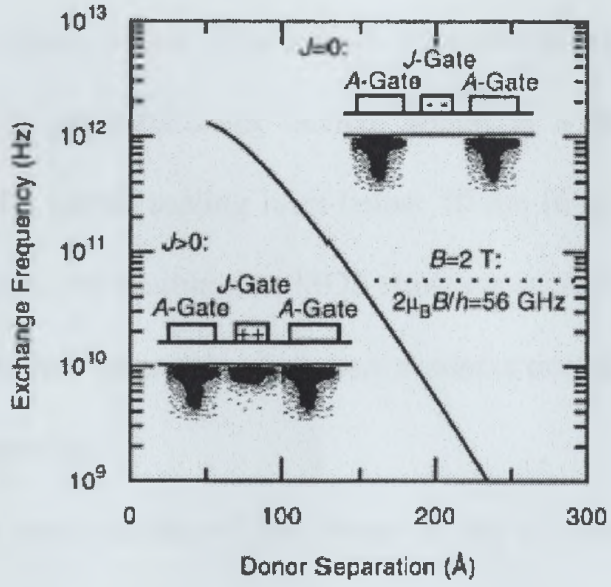


Fig. 1.3: J gates vary the electrostatic potentional (V) barrier between donors to enhance or reduce exchange coupling, proportional to electron wavefunction overlap. The exchange frequency, once the above mentioned potential (V) is zero, is plotted for Si [5].

Figure 1.4 summarizes the process done in a Kane device.

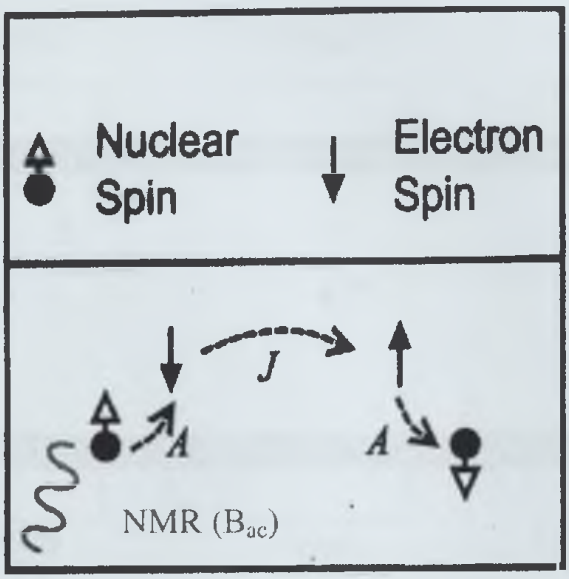


Fig. 1.4: Electron J-exchange-mediated nuclear spin A-interaction [5].

In this thesis, we propose a new structure to improve spin qubits operation with a double gate metal-oxide semiconductor device, which is a promising candidate for CMOS technologies with lateral scaling limit below 10 nm [6-8]. Specifically, we show by computer modeling that the double-gate MOS structure achieves a better control of the modulation of the hyperfine interaction between a conduction electron and the nuclear spin for single qubit operation.

Figure 1.5 shows a cross section of the device in the x-y plane with the coordinate system used in our model. The device has two sets of three n+ polysilicon gates at the top and at the bottom of the device. The central A-gates are 84 Å wide while the sides J-gates are 60 Å wide. All gates have a thickness of 145 Å in the y-direction. The thickness of

the SiO_2 layer is 3 nm. For simulation purposes, the device extensions in the x and z directions are 494 Å and 1034 Å, respectively. The impurity is located at the mid-vertical distance (y-direction) between the two A-gates.

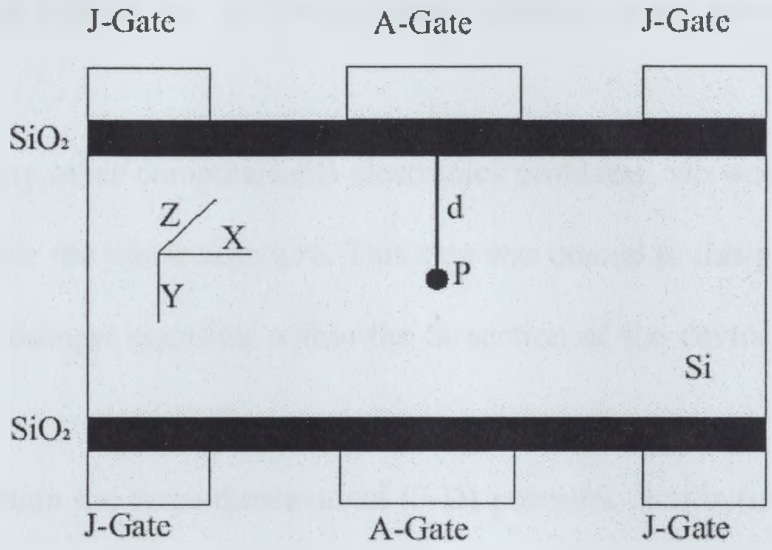


Fig. 1.5: Schematic cross section of the double gate device in the x-y plane along with the coordinate system.

CHAPTER 2

POTENTIAL DISTRIBUTION AND FLAT BAND

2.1 Modeling and Solving the 3D Electrostatic Potential in the Device

Similar to many other computational electronics problems, we were required to solve the potential within the whole structure. This step was crucial to this problem as we were to solve the Schrödinger equation within the Si section of the device. This was done in the 3D domain.

In order to obtain the three-dimensional (3-D) potential distribution and energy band diagram in the device under external gate biases, we first solved the Poisson equation

$$\nabla.(\varepsilon \nabla V) = -\rho \tag{2.1}$$

where V stands for the electrostatic potential, ε is the dielectric constant of the respective materials, i.e., Si or SiO_2, and $\rho(r)$ is the volume charge density in the whole structure.

Due to the singularity of the P-ion coulombic potential, we use a suitable pseudo-potential model which provides stable and accurate results in the iteration procedure used in solving Eq. (2.1). In this model, the hydrogenic pseudo-potential has a finite value at the impurity location and a 1/r-dependence at long distance [9]. It is parameterized to provide the ionization energy of P-donors in Si materials. However, because of the gate and oxide proximity, and the inherent anisotropy of the device, the model as such does not satisfy the MOS device boundary conditions. Therefore, by differentiating the pseudo-potential, we obtain the equivalent pseudo-charge that is used

as source term in Poisson's equation and solved with the Dirichlet boundary conditions on the top and bottom of the structure, whereas Neumann boundary conditions are used on the lateral surfaces.

$$-\frac{1}{r} \cong -\frac{1}{r} erf(\frac{r}{0.25}) + (-1.9287 + 0.3374r^2)\exp(-(\frac{r}{0.284})^2) \tag{2.2}$$

The following Figures 2.1 and 2.2 show the singularity along with the fit of the singularity and also the equivalent charge separately. As shown in Figure 2.1, the singularity does exist and this is a challenge in modeling (or there is no way to model it numerically in our code.). Nonetheless, the appropriate use of the expression above accompanied by some modeling techniques (and some tuning in convergence), we made it possible to solve some theoretically well understood problems to rederive confirmed data.

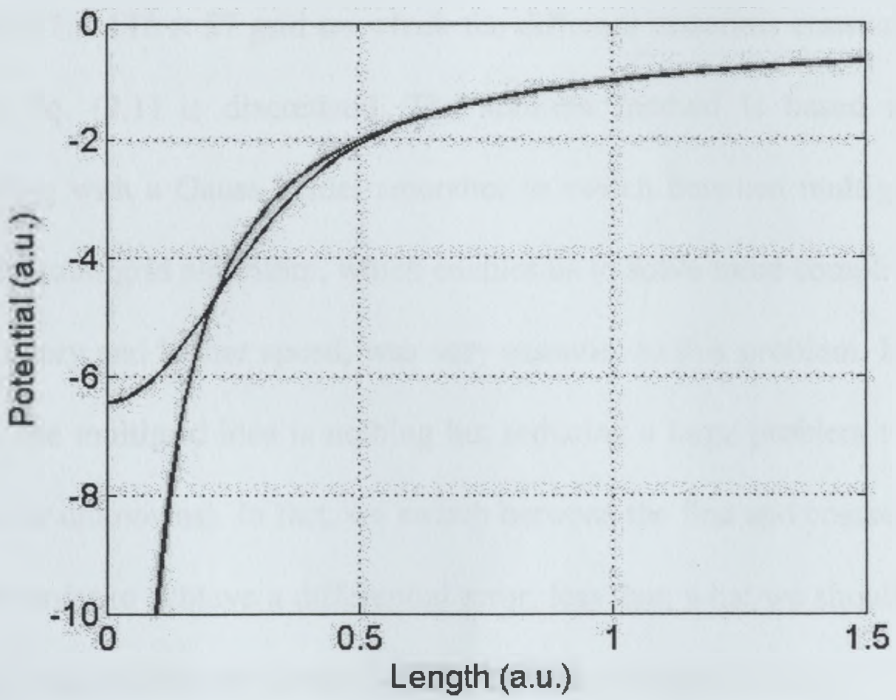


Fig. 2.1: Singularity removed by the use of appropriate Pseudo-Potential.

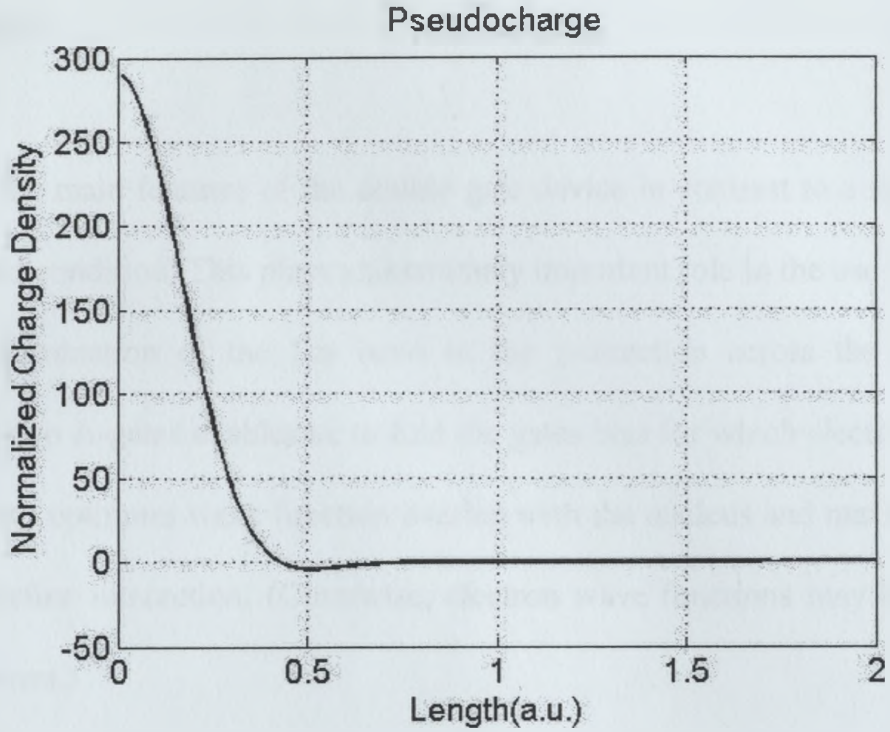


Fig. 2.2: The equivalent charge obtained from the Pseudo-Potential expression.

We used a 57 × 113 × 57 grid on which the different materials constant ε and m^* are defined and Eq. (2.1) is discretized. The solution method is based on a multigrid algorithm along with a Gauss-Seidel smoother to switch between multigrid levels [10]. The use of the multigrid algorithm, which enables us to solve more complicated problems with less memory and higher speed, was very essential to this problem. In fact, to put it very simply, the multigrid idea is nothing but reducing a large problem to a problem of fewer nodes (or unknowns). In fact, we switch between the fine and coarse grids over and over again in order to achieve a differential error, less than what we should expect in our result. In our code, mainly the Gauss-Seidel was doing this sort of duty.

2.2 Flat Band

One of the main features of the double gate device in contrast to a single gate one is the flat Band condition. This plays an extremely important role in the use of the device.

The determination of the flat band in the y-direction across the bisecting plane connecting two A-gates enables us to find the gates bias for which electrons sit on the P-impurity with optimum wave function overlap with the nucleus and maximum amplitude of the hyperfine interaction. (Otherwise, electron wave functions may leak towards the isolation layers.)

Previous 1-D formulation of the double gate MOS device has shown that the flat band voltage, in addition to the work function difference, is dependent on the thicknesses of both the Si and SiO_2 layers [11]. However, owing to 3D geometry of our devices, the flat band criterion is more complicated than in the single gate counterparts. Moreover, the innate symmetry of the device indicates a symmetric behavior of the wave function modulation with respect to the bias difference between the top and bottom gates. Because we are interested in the control of the electron wave function around the P-impurity by the A-gates, we focus on the flat band condition in the y-z plane at the impurity location.

Figure 2.3 shows the locus for flat band conditions in the $V_a - V_j$ diagram for three different Si layer thicknesses of 17.2 nm, 30.4 nm, and 43.6 nm, respectively. The diagram indicates two different flat regimes: For $V_a < -0.2$ V, flat band is achieved over the x-y plane when $V_a = V_j$; away from this condition, changing one of the gate voltages with respect to the other distorts the band in the x-y planes. For $V_a = -0.2$ V, flat band is only achieved underneath the A-gates, independently of the J-gate voltages (Figure 2.3,

inset). This particular V_a value corresponds to the work function difference between the n+ doped poly-Si A-gate and the Si-layer along with additional minor contributions of the charge distribution and size effects, which is the usual condition for flat band in MOS double gate transistor. However for $V_j > V_a$, flat band is only achieved in the y-z plane containing the impurity, underneath the A-gate where the potential energy exhibits a maximum along the x-direction; this situation is unstable for electrons since they tend to move toward lower potential energy regions beneath the J-gates. Therefore, in the present analysis we concentrate on flat band achieved for $V_a = V_j < -0.2$ V.

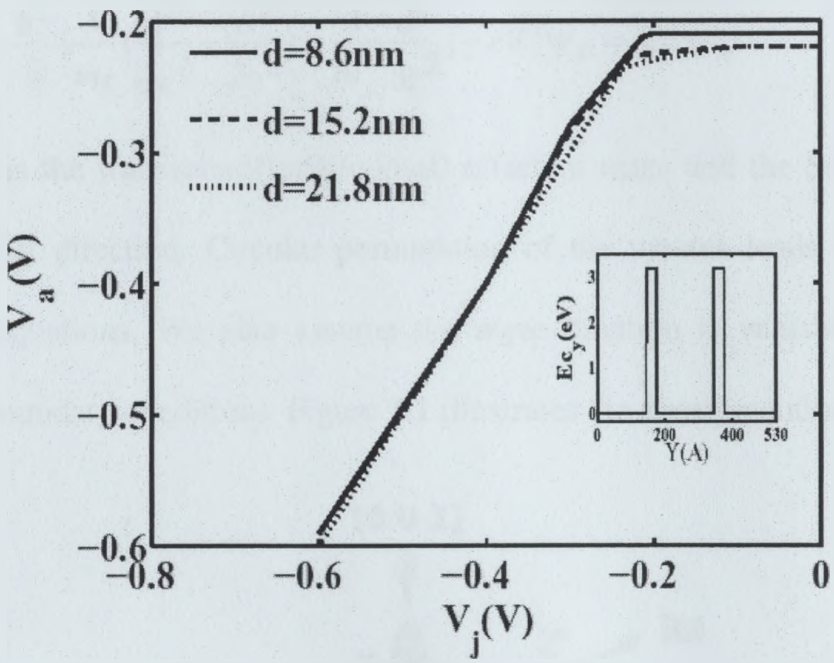


Fig. 2.3: V_a-V_j diagram for which flat band is achieved for three different impurity distances. (Inset shows the band diagram along the bisecting line of A gates.)

CHAPTER 3

FROM FLAT BAND TO SCHRÖDINGER EQUATION

3.1 Appropriate Form of Schrödinger Equation

Once the flat band conditions have been determined, we solve the effective mass Schrödinger equation in the presence of the P-impurity for each valley:

$$[-\frac{\hbar^2}{2}[\frac{1}{m_t}(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2})+\frac{1}{m_l}\frac{\partial^2}{\partial z^2}]-eV]\Psi_n = E_n\Psi_n \qquad (3.1)$$

Here m_t (m_l) is the transverse (longitudinal) effective mass and the Si-layer is oriented along the [100] direction. Circular permutation of the masses leads to a set of three independent equations. We also assume the wave function is vanishing at the device boundaries (boundary condition). Figure 3.1 illustrates the above mentioned point.

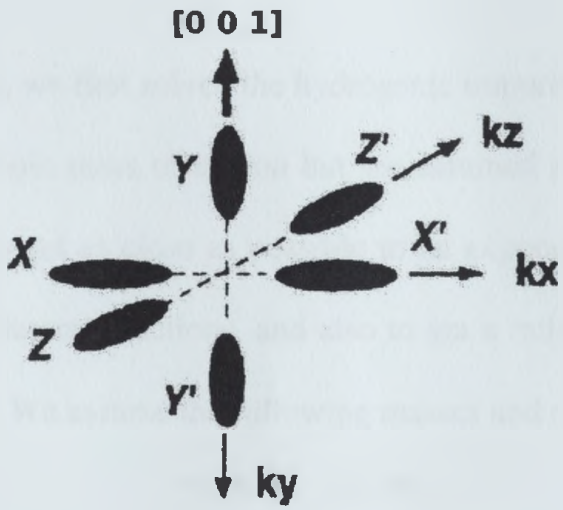


Fig. 3.1: Orientation of the six doubly degenerated conduction-band valleys in reciprocal space for Si.

3.2 IEOM Method

In solving the eigenvalues of Eq. (3.1), we use the IEOM algorithm [12] which has the ability to generate an arbitrary number of eigenstates and it scales as NE^2 * NG, where NE is the number of eigenstates and NG ($57 \times 91 \times 57$) is the number of grid points (for Silicon layer only), as opposed to the NG^3 for other conventional eigenvalue solvers. Since the number of eigenstates required is by far less than the number of grid points, this method is less exhaustive of memory and CPU time. The central idea of this method comes from the 'time evolution' in quantum mechanics. In fact, the appropriate use of the equations pertinent to that part, leads to a method in order to simultaneously solve the wave function in 3D along with appropriate eigenvalues of each state. The only shortcoming of the method is related to handling degenerate states. Interested readers are referred to the reference above for further information on this method.

3.3 Results

In order to test the code, we first solved the hydrogenic impurity problem. In this case, we considered the anisotropic mass of silicon but we assumed a whole bulk of it. This way, we were expecting to get as close as possible to an exponential solution, but with different decay rates at different directions, and also to get a rational value of ionization for a hydrogenic impurity. We assume the following masses and dielectric constant:

$$m_x = m_y = 0.19 m_e$$

$$m_z = 0.92 m_e$$

$$\varepsilon_r = 11.7$$

where m_e is electron rest mass. The domain size is a box of 1110A × 1110A × 1110A to allow sufficient decay of the electron wavefunction. Figures 3.2 and 3.3 show the results achieved for this problem.

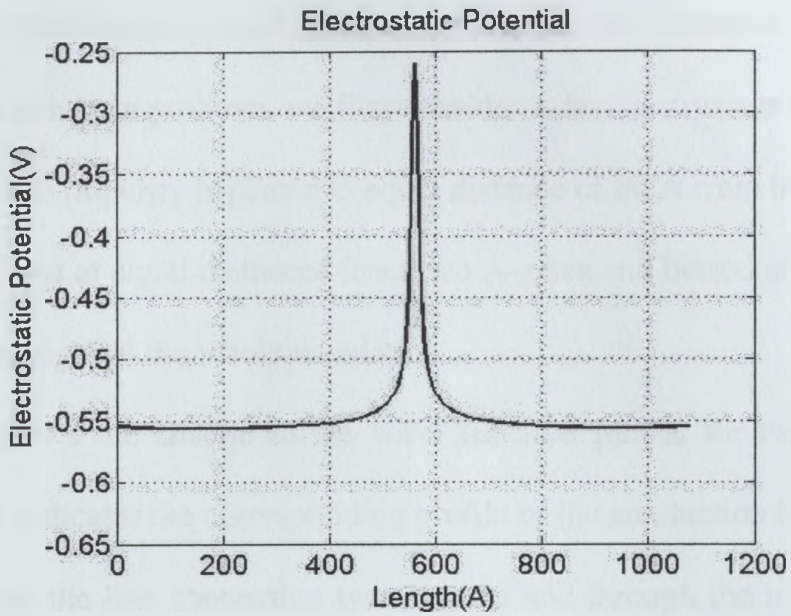


Fig. 3.2: The electrostatic potential obtained in this problem.

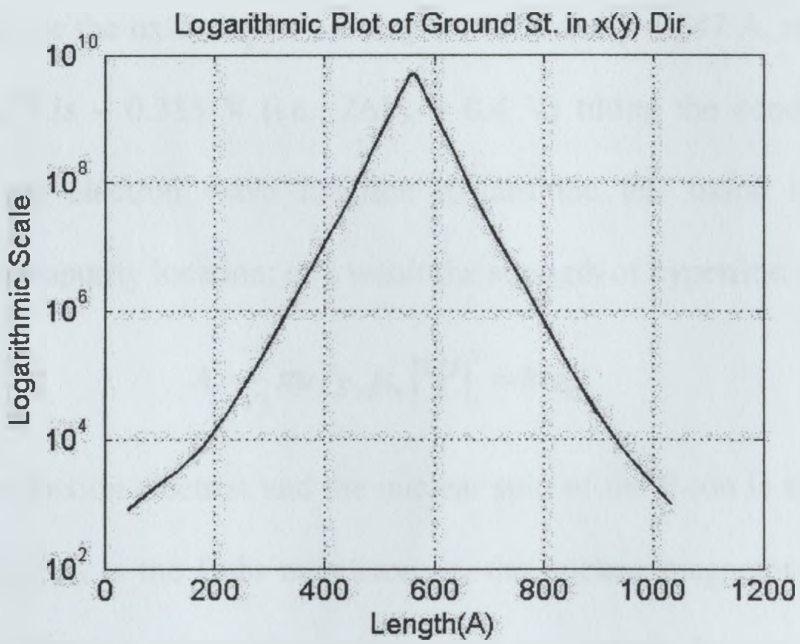


Fig. 3.3: The logarithmic plot of wavefunction in x(y) directions.

The ionization energy found for this problem is – 31.954 meV, where in theory it is – 31.27 meV. As Figure 3.3 shows, the logarithmic scale is linear, which indicates the original wavefunction is exponential, as expected in the case of a hydrogenic impurity. The deflections from linearity are due to size effects and box (domain) limitations.

Returning to our main problem, we first consider a device structure with a Si thickness of 172 Å where the impurity is placed at equal distance of 86 Å from both oxide layers; J-gates are positioned at equal distances from two A-gates and biased at the constant value of – 0.562 V throughout the whole simulation.

Figure 3.4 shows the change in the wave function profile for two different A-gate biases; the inset indicates the corresponding profile of the conduction band edge along the y-direction across the line connecting two A-gates and through the impurity. In the first case (V_a = – 0.555 V; $2\Delta V_a = V_a^{top} - V_a^{bott} = 0$) the device is under flat band condition with the maximum of the electron wave function on the impurity, located at y = 261 Å. (On the figure scale the oxide layers are at y = 145 Å and y = 347 Å, respectively.) In the second case V_a^{top} is – 0.355 V (i.e., $2\Delta V_a$ = 0.4 V) tilting the conduction band edge, which moves the electron wave function toward the left oxide layer, reducing its amplitude at the impurity location; as a result the strength of hyperfine interaction

$$A = \frac{8}{3}\pi\mu_B g_n \mu_n \left|\Psi\right|_I^2 = \hbar\omega_{hf} \tag{3.2}$$

between the conduction electron and the nuclear spin of the P-ion is also reduced. In the above expression, μ_B is the Bohr magneton, μ_n the nuclear magneton, g_n the nuclear g-factor, A the hyperfine interaction energy, and ω_{hf} stands for the nuclear magnetic resonance (NMR) frequency for spin rotation [5]. The fact that the area under the curves is unequal from this cross-sectional plot of the wave functions indicates a spreading of

the wave function in the x-z plane when pulled towards the gate (contrary to flat band in which the wave function has an ellipsoidal symmetry).

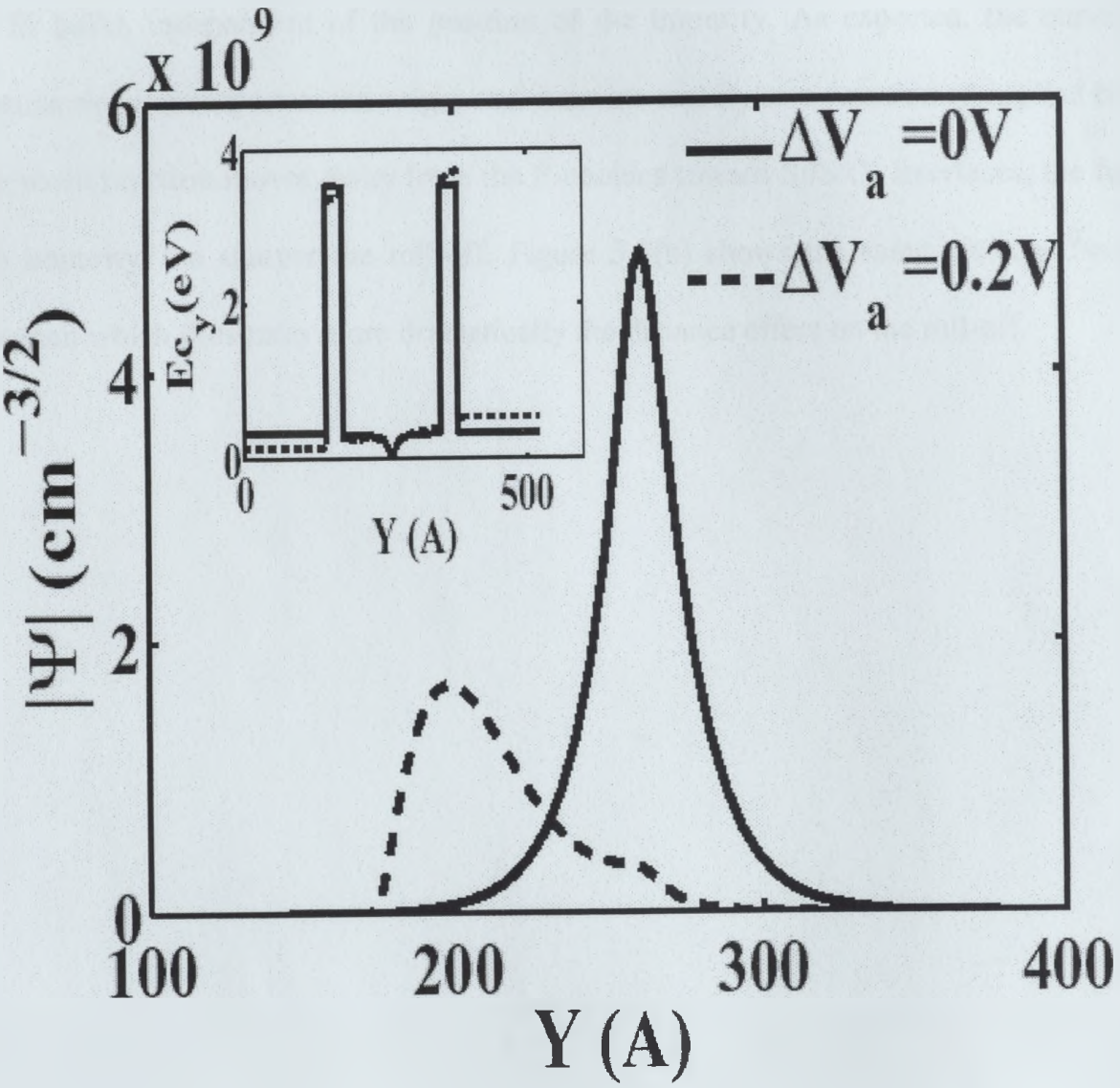
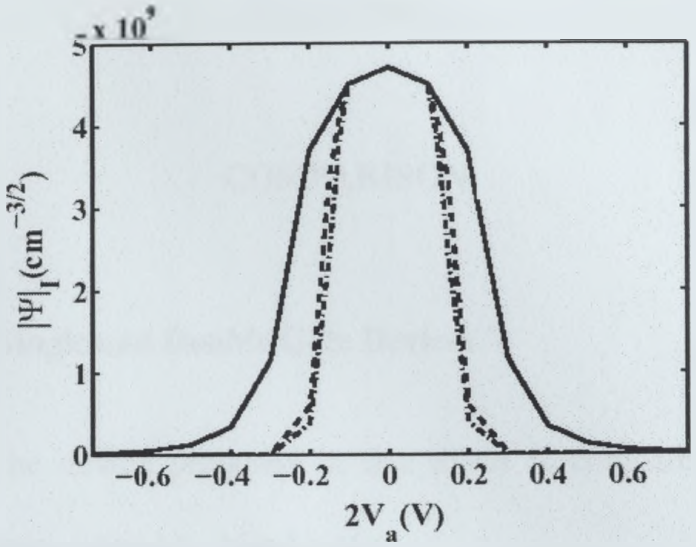


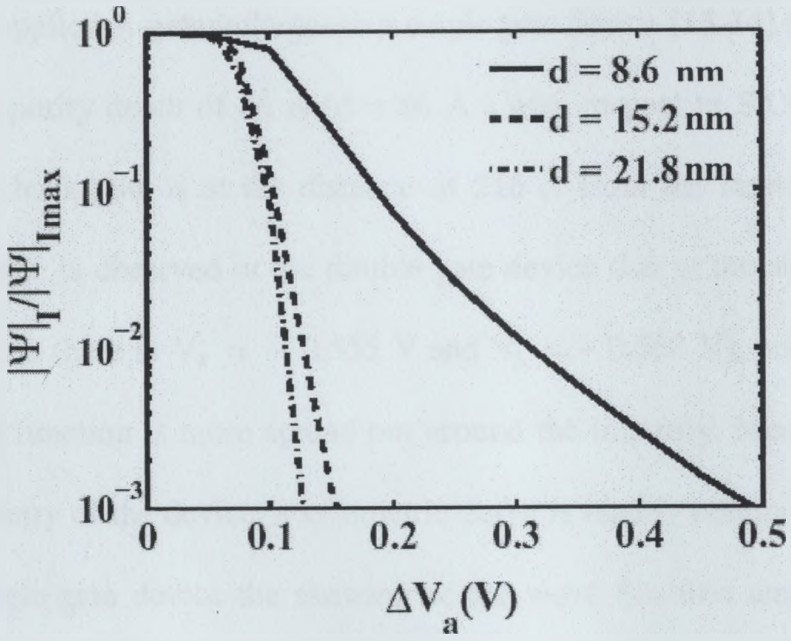
Fig. 3.4: Profile of the electron wave function along the bisecting line of A-gates for two values of the applied voltage $V_a = -0.555$ V (flat band, $\Delta V_a = 0$) and $\Delta V_a = 0.2$ V. [Inset: Conduction band profile in the y direction along the bisecting line of A-gates for two different ΔV_a values (impurity depth = 86 Å) in smaller scale plot.]

Figure 3.5(a) shows the variation of the wave function amplitude at the impurity location for different impurity distances, as a function of A-gate biases while J-gate

biases are kept constant. For each impurity distance, the origin of the horizontal scale corresponds to the flat band condition $V_a = V_j < -0.2$ V for which the wave function amplitude is very close to the bulk value (which implies an NMR frequency close to that of Si bulk), independent of the position of the impurity. As expected, the curves are symmetric with respect to the origin and decrease rapidly as a function of applied bias as the wave function moves away from the P-nucleus toward Si/SiO_2 interfaces; the further the impurity, the sharper the roll-off. Figure 3.5(b) shows the same plot on [10]semilog diagram which illustrates more dramatically the distance effect on the roll-off.



(a)



(b)

Fig. 3.5(a): Amplitudes of the wave function on the impurtiy for three different impurity distances from the SiO_2 layers. Flat band conditions for 86 Å , 152 Å, and 218 Å are respectively (V_a = – 0.555 V, V_j = – 0.562 V), (V_a = – 0.5915 V , V_j = – 0.6 V), and (V_a = – 0.5 V, V_j = – 0.5 V). (b): Logarithmic scale plot of the same curves, normalized to their maximum values.

CHAPTER 4

COMPARISON

4.1 Comparison of Single and Double Gate Devices

In this chapter, the device proposed in this thesis is compared to work done by previous students in our group, i.e., Min Lu et al.

Figure 4.1 shows the variation of the wave function amplitude at the impurity position as a function of applied A-gate voltages in a single gate device [13-14] and in double gate device for an impurity depth of 86 Å (d = 86 Å) with respect to SiO_2 layers. In single gate device, the back gate is at the distance of 216 Å from the impurity. Larger wave function magnitude is observed in the double gate device due to the ability of achieving flat band condition (here at $V_a = -0.555$ V and $V_j = -0.562$ V), unlike in single gate device the wave function is more spread out around the impurity. Moreover, because of the innate symmetry of the device, a symmetric curve is readily obtained in the structure, while in the single gate device the skewing of the wave function amplitude to the left (negative voltages) indicates the abrupt leakage of the wave function toward the substrate, away from the Si/SiO_2 interface.

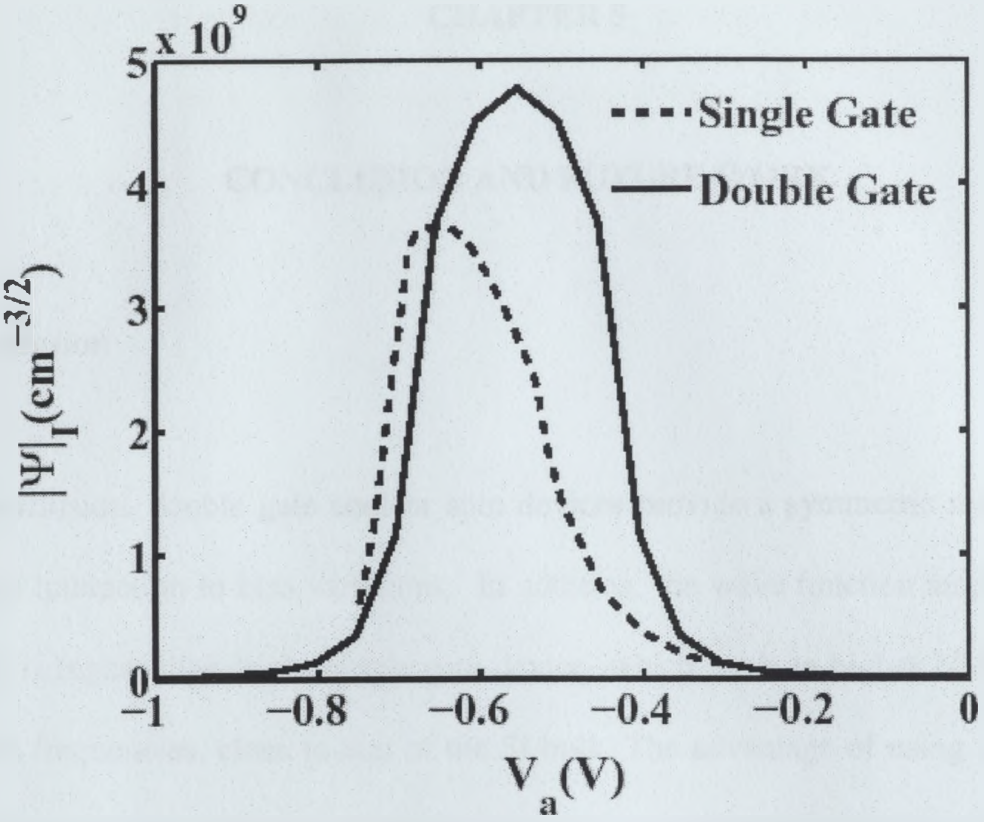


Fig. 4.1: Comparison of wave function amplitude variations with A-gate voltages for single and double gate devices (impurity depth = 86 Å).

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In conclusion, double gate nuclear spin devices provide a symmetric response of the hyperfine interaction to bias variations. In addition, the wave function amplitude on the impurity is higher than in the single gate device, which leads to higher NMR spin-qubit operation frequencies, close to that of the Si bulk. The advantage of using a double gate structure is that flat band can always be achieved regardless of the impurity depth with corresponding hyperfine interaction energy values close to that of the bulk; hence, for single spin rotation the device can be best biased around its flat band value with the appropriate J and A gates variations, which prevents the electron wave function moving away from the P-nucleus active region.

5.2 Future Work

As a suggestion for future work, computationally one can focus on self-consistent effects of the device simulation. The point this simulation is missing is the fact that we did not take into account the self consistent effects and also many body effects like the entire DFT (i.e., density functional theory potentials) considerations. Considering these effects would require a more advanced code and most probably parallel programming

techniques which were missing due to lack of time in this project. Moreover, other interesting features of the device like currents and periodic boundary effects can also be incorporated into the code. Figure 5.1 shows the algorithm for a DFT code.

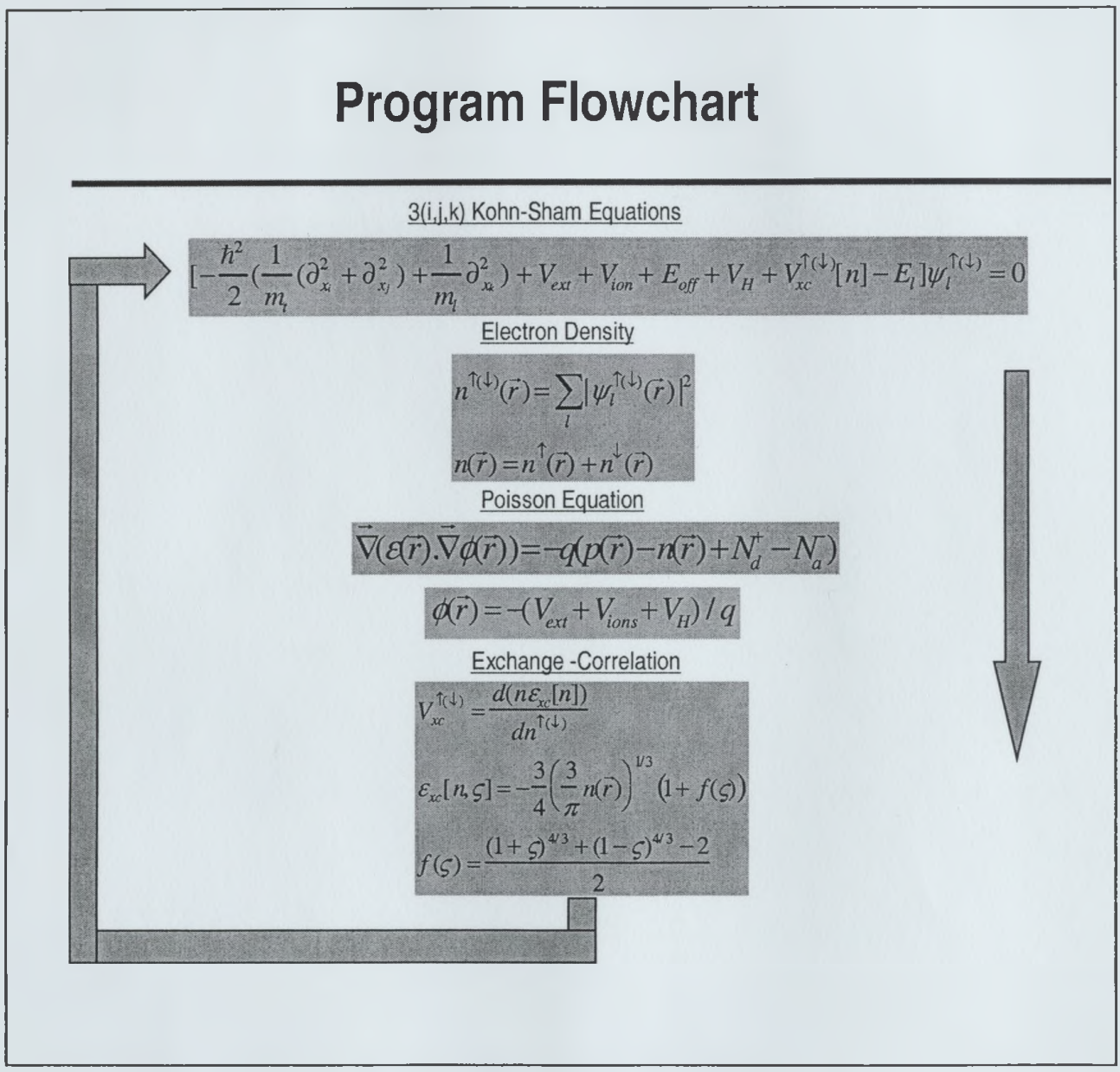


Fig. 5.1: DFT program flow chart.

As for experimental attempts, one may be able to fabricate and test the device to see how environmental effects can play roles in the performance of the device. Accordingly,

one may adjust the code to take into the account the modelling of the environmental effects.

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